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US9312838B2	Specification Support	Xilinx UltraScale FPGA (including but not limited to Kintex FPGAs and Virtex FPGAs) Clocking Resources (The accused instrumentality)
1Pre. An apparatus, comprising: **1a.** first and second clocks operable to generate first and second input clock signals, respectively, wherein the first and second input clock signals are asynchronous in relation to one another;	The disclosed embodiments may be implemented in a telecommunication system where module 110 transmits two asynchronous clock signals to module 120 over conductor 130. Module 110 may be a CPU module and module 120 may be a peripheral module. Although, FIG. 1 illustrates transfer of two clock signals between only two modules, **the disclosed embodiments can be implemented for transferring two clock signals** among three or more modules.	The accused instrumentality consists of an apparatus comprising first and second clocks operable to generate first and second input clock signals, respectively, wherein the first and second input clock signals are asynchronous in relation to one another. The Xilinx UltraScale Arhitecture governs the design and function of Xilinx FPGAs of the Kintex and Virtex families. This includes FPGAs like KU025, KU035, KU040, VU065, VU080, VU095 and **many more**. [See Fig. 1] The Xilinx UltraScale Architecture clock resources manage complex and simple clocking requirements. The clock management tiles (CMT) are used to provide clock frequency synthesis, deskew, and jitter filtering functionality. In the Xilinx UltraScale architecture-based devices, the CMT comprises a mixed-mode clock manager (MMCM) and two phase-locked loops (PLLs). The MMCMs function as frequency synthesizers, and jitter filters for either internal/external clocks and deskew clocks. See Fig. 2.

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	Referring again to FIG. 1, **module 110 includes clocks 102 and 104 which generate clock signals 106 and 108, respectively**. Clock signal 106 may be synchronized to an external network clock while clock signal 108 may not be synchronized to the external network clock (i.e. free-run clock signal or synchronized to a different external network). **Thus, clock signals 106 and 108 are asynchronous with respect to one another.** [Col.4, Lines 23-39]	**Citation 1: Xilinx FPGA families using the UltraScale Architecture** *Table 1:* **Device Resources** Fig. 1 Source: https://www.xilinx.com/support/documentation/data_sheets/ds890-ultrascale-overview.pdf, Page 1, Last accessed on July 28, 2020, Exhibit B

	Kintex UltraScale FPGA	Kintex UltraScale+ FPGA	Virtex UltraScale FPGA	Virtex UltraScale+ FPGA	Zynq UltraScale+ MPSoC	Zynq UltraScale+ RFSoC
MPSoC Processing System					✓	✓
RF-ADC/DAC						✓
SD-FEC						✓
System Logic Cells (K)	318–1,451	356–1,843	783–5,541	862–8,938	103–1,143	678–930
Block Memory (Mb)	12.7–75.9	12.7–60.8	44.3–132.9	23.6–94.5	4.5–34.6	27.8–38.0
UltraRAM (Mb)		0–81		90–360	0–36	13.5–22.5
HBM DRAM (GB)				0–16		
DSP (Slices)	768–5,520	1,368–3,528	600–2,880	1,320–12,288	240–3,528	3,145–4,272
DSP Performance (GMAC/s)	8,180	6,287	4,268	21,897	6,287	7,613
Transceivers	12–64	16–76	36–120	32–128	0–72	8–16
Max. Transceiver Speed (Gb/s)	16.3	32.75	30.5	58.0	32.75	32.75
Max. Serial Bandwidth (full duplex) (Gb/s)	2,086	3,268	5,616	8,384	3,268	1,048
Memory Interface Performance (Mb/s)	2,400	2,666	2,400	2,666	2,666	2,666
I/O Pins	312–832	280–668	338–1,456	208–2,072	82–668	280–408

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		Citation 2: Clock Management Tile **Overview** In UltraScale™ architecture-based devices, the clock management tile (CMT) includes a mixed-mode clock manager (MMCM) and two phase-locked loops (PLLs). The main purpose of the PLL is to generate clocking for the I/Os. But it also contains a limited subset of the MMCM functions that can be used for general clocking purposes. Fig. 2 Source: https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf, Page 35, Last accessed on July 26, 2020, Exhibit A The MMCM architecture comprises two input multiplexers that select a first input clock (input or reference clock; CLKIN1 or CLKIN2) signal and a second input clock (feedback clock; CLKFB or CLKFBOUT) signal. The MMCM block diagram shown below also comprises a PLL (blocks PFD to VCO). The phase-frequency detector (PFD) in the PLL is is equipped to compare two asynchronous signals (i.e two signals with variable phase and frequency difference). Hence, both of the input clock signals are asynchronous relative to each other. See Fig. 3 and Fig. 4.

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Citation 3: MMCM Block Diagram

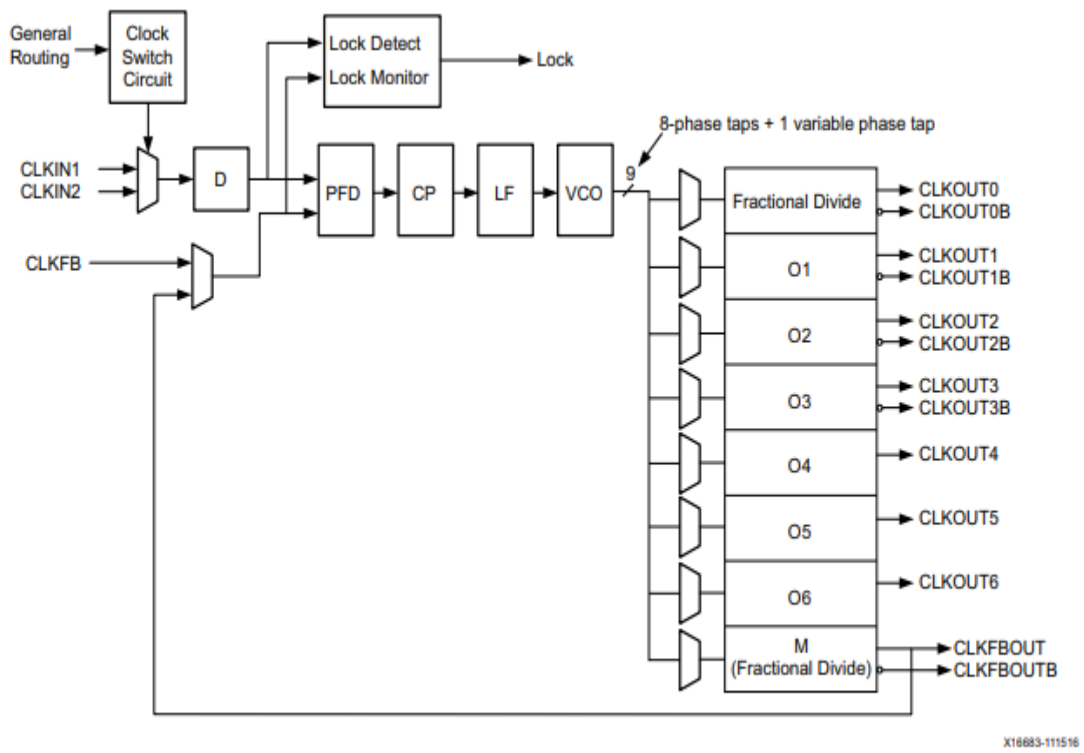

Figure 3-1: **Detailed MMCM Block Diagram**

Fig. 3

Source: https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf, Page 35, Last accessed on July 26, 2020, Exhibit A

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		Citation 4: Input (reference) clock and feedback clock Input multiplexers select the reference and feedback clocks from either the global clock I/Os or the clock routing or distribution resources. Each clock input has a programmable counter divider (D). The phase-frequency detector (PFD) compares both phase and frequency of the rising edges of both the input (reference) clock and the feedback clock. If a minimum High/Low pulse is maintained, the duty cycle is ancillary. The PFD is used to generate a signal proportional to the phase and frequency between the two clocks. This signal drives the charge pump (CP) and loop filter (LF) to generate a reference voltage to the VCO. The PFD produces an up or down signal to the charge pump and loop filter to Fig. 4 Source: https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf, Page 35, Last accessed on July 26, 2020, Exhibit A
1b. a first edge detector configured to receive the first input clock signal, the first edge detector operable to detect a rising edge of the first input clock signal and to generate a first enable signal;	FIG. 2 illustrates a block diagram of dual reference clock generator 112 according to various disclosed embodiments. **Clock generator 112 includes edge detector 202 configured to detect a rising edge of clock signal 106**, and in response edge	The accused instrumentality comprises a first edge detector configured to receive the first input clock signal, the first edge detector operable to detect a rising edge of the first input clock signal and to generate a first enable signal. The MMCM comprises of two input MUXes (Multiplexers) that serve as edge detectors (i.e., asynchronous MUX). See Fig. 5 and Fig. 6. Each edge detector receives an input clock signal (select line 'S') and detects a rising edge of that input clock signal to generate enable signals (Clock output of the asynchronous MUX).

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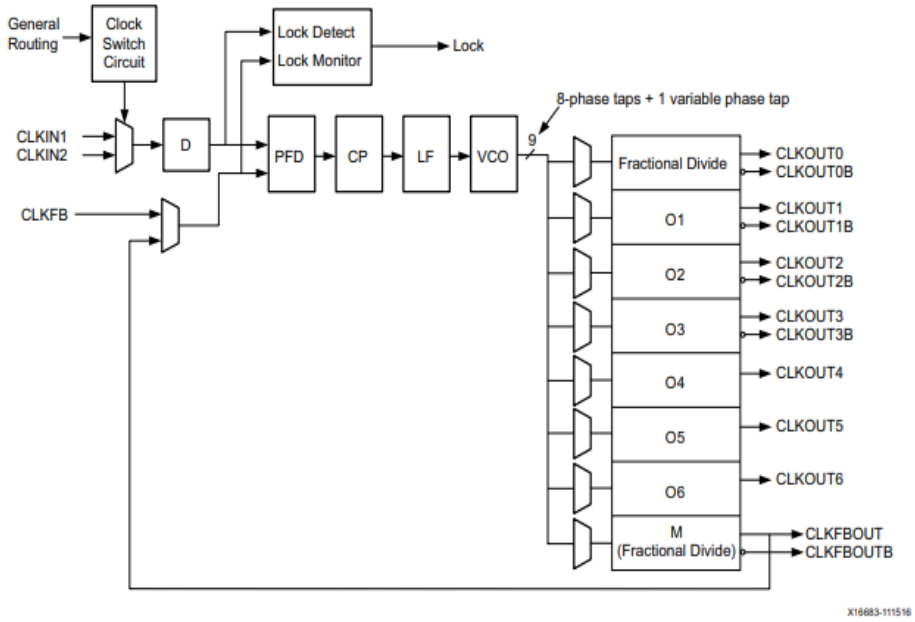
	detector 202 generates first enable signal 204. [Col.4, Lines 60-64]	Each MUX comprises of two input signals and a select line. The asynchronous MUX timing diagram of Fig. 7 shows that before the S line transitioned from low to high, I_0 was selected to be the output signal 'O'. When the S line transitioned from low to high (i.e., rising edge of the clock was detected), I_1 was selected to be the output signal 'O', and thus a first clock signal was enabled. **Citation 5: Input MUXes**  *Figure 3-1:* **Detailed MMCM Block Diagram** Fig. 5

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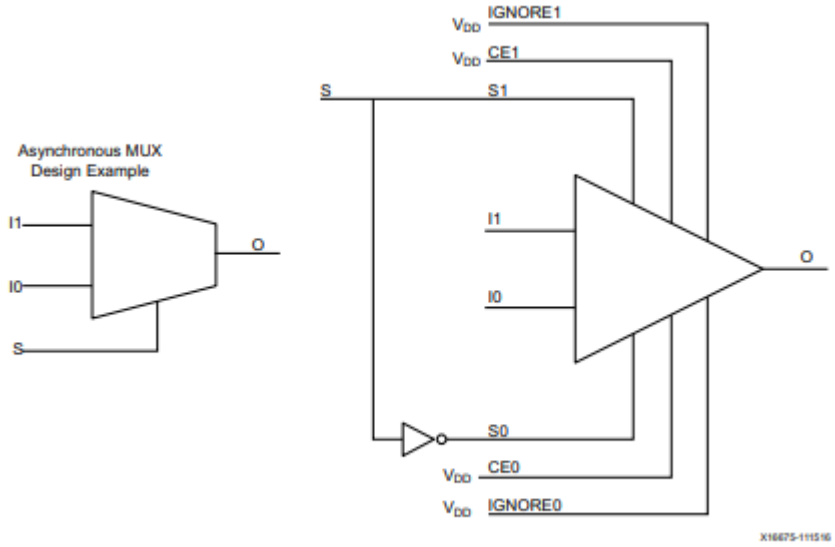
		Source: https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf, Page 35, Last accessed on July 26, 2020, Exhibit A **Citation 6: Asynchronous MUX**  *Figure 2-14:* **Asynchronous MUX with BUFGCTRL Design Example** Fig. 6 Source: https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf, Page 21, Last accessed on July 26, 2020, Exhibit A

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Citation 7: Asynchronous MUX Timing Diagram

Figure 2-15 shows the asynchronous MUX timing diagram.

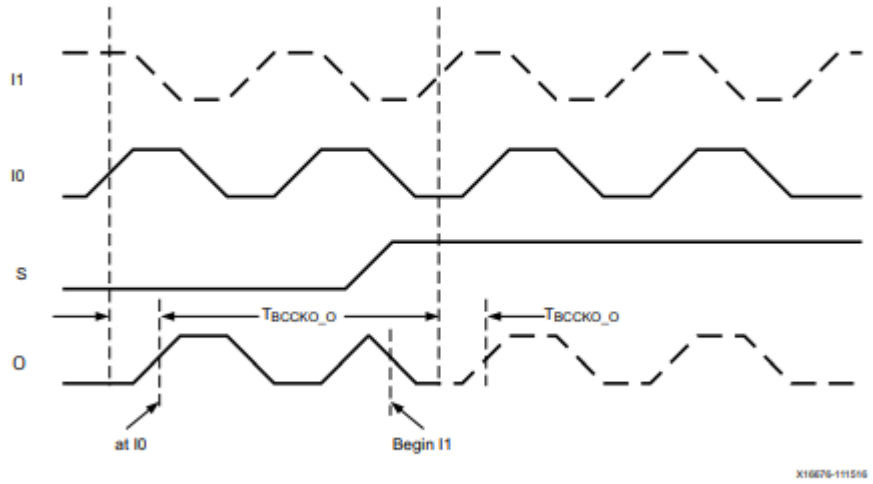

Figure 2-15: **Asynchronous MUX Timing Diagram**

Fig. 7

Source: https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf, Page 22, Last accessed on July 26, 2020, Exhibit A

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1c. a second edge detector configured to receive the second input clock signal, the second edge detector operable to detect the rising edge of the second input clock signal and to generate a second enable signal;	Clock generator 112 also includes **edge detector 206 configured to detect a rising edge of clock signal 108**, and in response edge detector generates second enable signal 208. [Col. 4, Line 65-67] In block 612, **the second enable signal is generated responsive to a detection of a rising edge of the second input clock signal**. In block 616, the reference clock signal is generated responsive to the first and second enable signals, wherein the reference clock signal is representative of	The accused instrumentality comprises a second edge detector configured to receive the second input clock signal, the second edge detector operable to detect the rising edge of the second input clock signal and to generate a second enable signal. The MMCM comprises of two input MUXes (Multiplexers) that serve as edge detectors (i.e., asynchronous MUX). See Fig. 8and Fig. 9. Each edge detector receives an input clock signal (select line 'S') and detects a rising edge of that input clock signal to generate enable signals (Clock output of the asynchronous MUX). Each MUX comprises of two input signals and a select line. The asynchronous MUX timing diagram of Fig. 10shows that before the S line transitioned from low to high, I_0 was selected to be the output signal 'O'. When the S line transitioned from low to high (i.e., rising edge of the clock was detected), I_1 was selected to be the output signal 'O', and thus a first clock signal was enabled.

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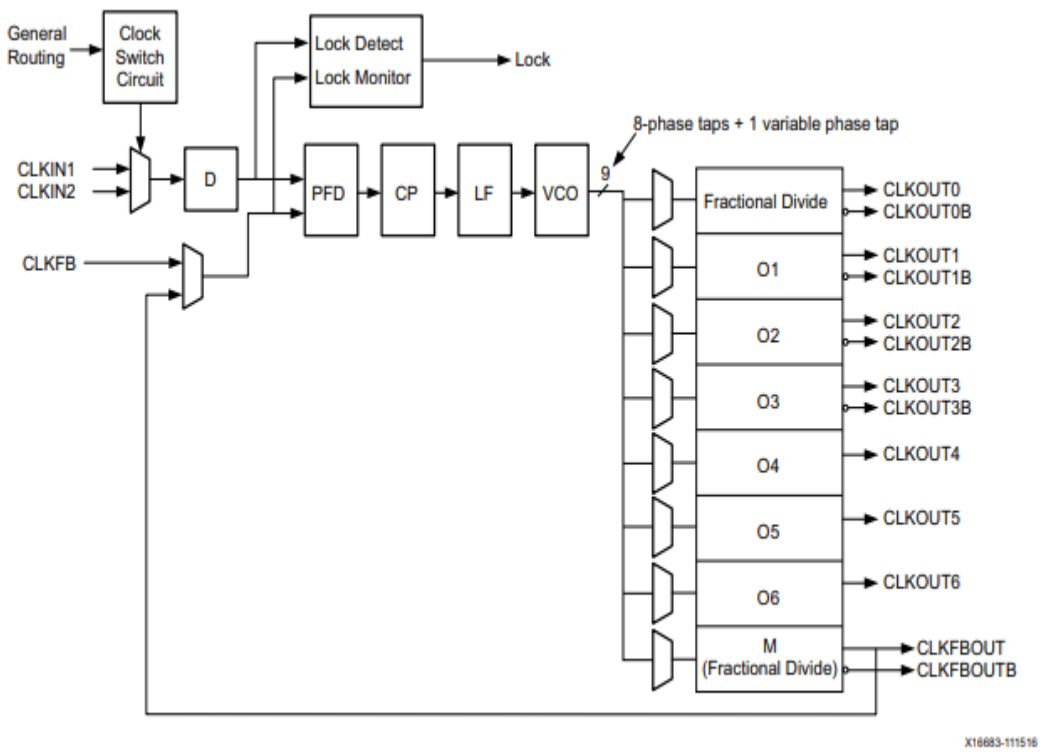
	the first and second enable signals. [Col. 6, Lines 17-22]	**Citation 8: Input MUXes**  *Figure 3-1:* **Detailed MMCM Block Diagram** Fig. 8 Source: https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf, Page 35, Last accessed on July 26, 2020, Exhibit A

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Citation 9: Asynchronous MUX

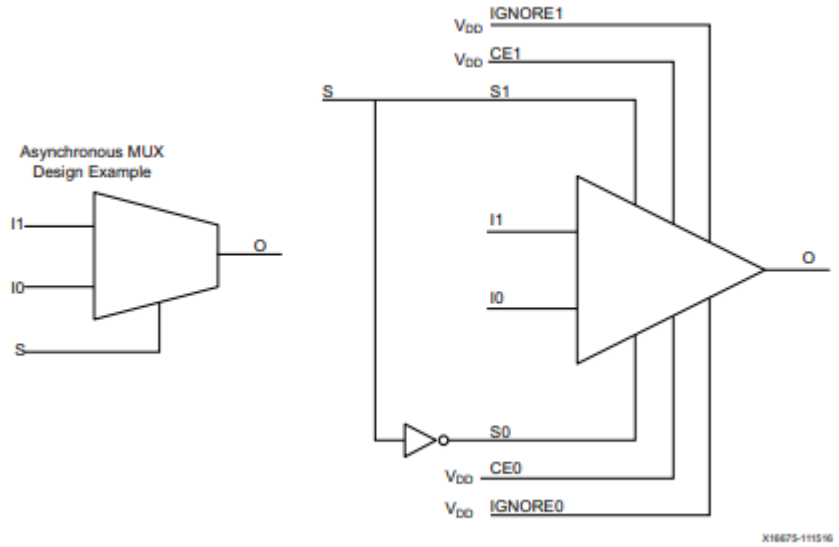

Figure 2-14: **Asynchronous MUX with BUFGCTRL Design Example**

Fig. 9

Source: https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf, Page 21, Last accessed on July 26, 2020, Exhibit A

Citation 10: Asynchronous MUX Timing Diagram

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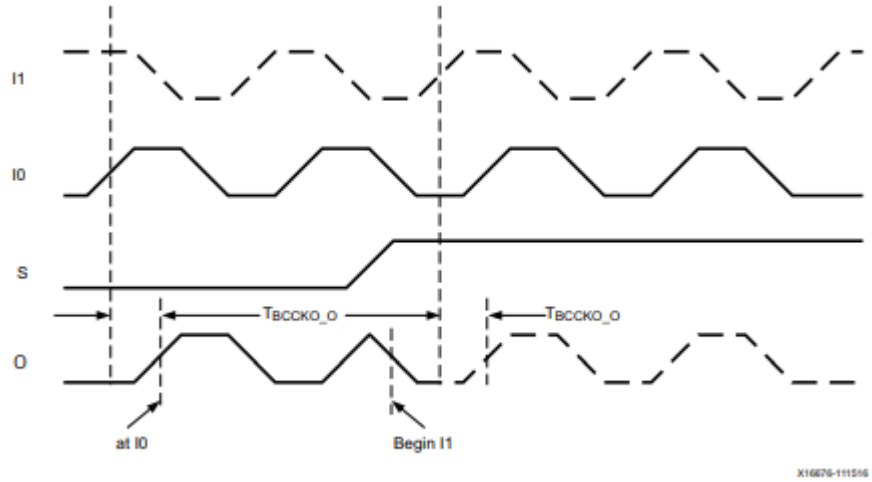
		Figure 2-15 shows the asynchronous MUX timing diagram.  *Figure 2-15:* **Asynchronous MUX Timing Diagram** Fig. 10 Source: https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf, Page 22, Last accessed on July 26, 2020, Exhibit A
1d. a first divider configured to receive the first enable signal and operable to generate a first adjusted enable signal	Clock generator 112 also includes counter 212 (or divider) configured **to receive first enable signal 204. Counter 212 delays first enable signal 204 by a**	The accused instrumentality comprises a first divider configured to receive the first enable signal and operable to generate a first adjusted enable signal based on a first predetermined factor. In the MMCM architecture, the clock output signal (i.e. first enable signal) from one of the two BUFGMUX is connected to a counter divider 'D' (i.e., first divider). The counter divider ('D') is

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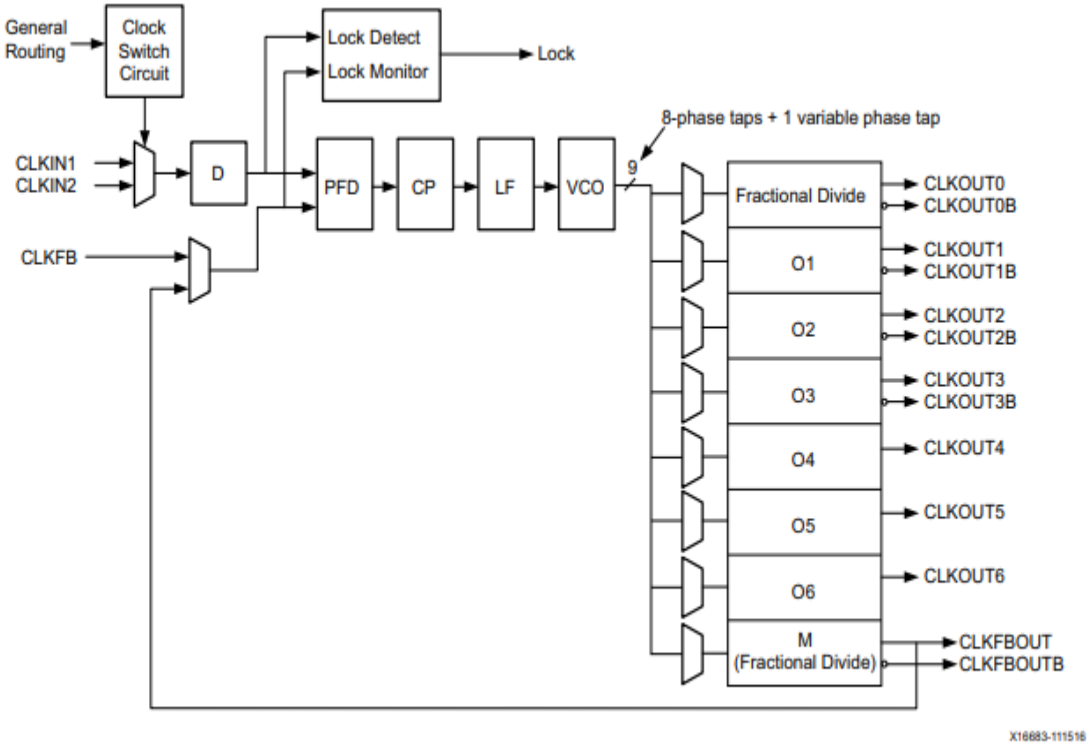
based on a first predetermined factor; and	**predetermined time period and generates first adjusted enable signal 216**. [Col. 5, Lines 1-4] According to disclosed embodiments, **counter 212 (or divider) converts the frequency of first enable signal 204 to 12.5 MHz**. Consequently, first adjusted enable signal 216 and second enable signal 208 have respective frequencies that are approximately close to one another. [Col. 5, Lines 26-31]	thus configured to receive the clock output signal (i.e. first enable signal). See Fig. 11 and Fig. 12. The output generated from the counter divider 'D' is a first adjusted enable signal. The factor 'D' using which the counter divider operates is the 'first predetermined factor'. **Citation 11: Counter Divider (D)**  *Figure 3-1:* **Detailed MMCM Block Diagram**

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		Fig. 11 Source: https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf, Page 35, Last accessed on July 26, 2020, Exhibit A **Citation 12: Counter Divider (D)** Input multiplexers select the reference and feedback clocks from either the global clock I/Os or the clock routing or distribution resources. Each clock input has a programmable counter divider (D). The phase-frequency detector (PFD) compares both phase and Fig. 12 Source: https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf, Page 35, Last accessed on July 26, 2020, Exhibit A
1e. a dual clock generator configured to receive the first adjusted enable signal and the second enable signal, and in response operable to generate a reference clock signal and transmit the reference	According to disclosed embodiments**, first adjusted enable signal 216 and second enable signal 208 are received by reference generator 218. Reference generator 218 generates reference clock signal 116 responsive to**	The accused instrumentality comprises a dual clock generator configured to receive the first adjusted enable signal and the second enable signal, and in response operable to generate a reference clock signal and transmit the reference clock signal over a single conductor. The first adjusted enable signal and the second enable signal that are output from the counter divider 'D' and a second MUX 'BUFGMUX', respectively, are sent to a dual clock generator module (i.e., blocks from PFD to VCO). The phase-frequency detector (PFD) generates a signal proportional to

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clock signal over a single conductor.	**first adjusted enable signal 216 (forcing rising edges on reference clock) and second enable signal 208 (forcing falling edges on reference clock).** Reference clock signal 116 is transmitted to module 120 over conductor 130. [Col. 3, Lines 32-39]	the phase and frequency of both the enable signals. The PFD produces an up or down signal to the charge pump (CP) and loop filter (LF) to determine whether the voltage-controlled oscillator (VCO) should operate at a higher or lower frequency. See Fig. 13 and Fig. 14. Eight signals can eventually be sent out from the VCO and one of those signals is the reference clock signal (i.e., CLKOUT) which is then transmitted forward over a single conductor as shown in Fig. 13.

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Citation 13: Dual Clock Generator

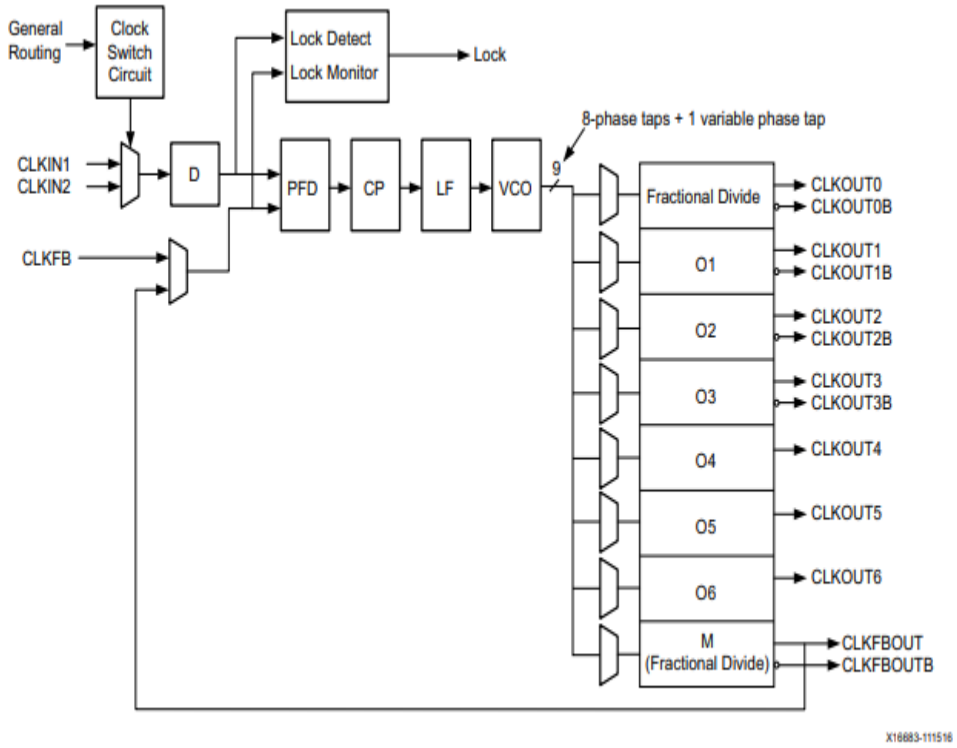

Figure 3-1: **Detailed MMCM Block Diagram**

Fig. 13

Source: https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf, Page 35, Last accessed on July 26, 2020, Exhibit A

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		Citation 14: Generating a reference clock signal Input multiplexers select the reference and feedback clocks from either the global clock I/Os or the clock routing or distribution resources. Each clock input has a programmable counter divider (D). The phase-frequency detector (PFD) compares both phase and frequency of the rising edges of both the input (reference) clock and the feedback clock. If a minimum High/Low pulse is maintained, the duty cycle is ancillary. The PFD is used to generate a signal proportional to the phase and frequency between the two clocks. This signal drives the charge pump (CP) and loop filter (LF) to generate a reference voltage to the VCO. The PFD produces an up or down signal to the charge pump and loop filter to determine whether the VCO should operate at a higher or lower frequency. When VCO operates at a frequency that is too high, the PFD activates a down signal causing the control voltage to be reduced, thus decreasing the VCO operating frequency. When the VCO operates at a frequency that is too low, an up signal increases voltage. The VCO produces eight output phases and one variable phase for fine-phase shifting. Each output phase can be selected as the reference clock to the output counters (Figure 3-1). Each counter can be independently programmed for a given customer design. A special counter M is also provided. This counter controls the feedback clock of the MMCM, allowing a wide range of frequency synthesis. Fig. 14 Source: https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf, Page 35-36, Last accessed on July 26, 2020, Exhibit A

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References Cited

Exhibit (s)	Description	Link
Exhibit A	Xilinx UltraScale Architecture Clocking Resources	https://www.xilinx.com/support/documentation/user_guides/ug572-ultrascale-clocking.pdf
Exhibit B	Xilinx UltraScale Architecture Products	https://www.xilinx.com/support/documentation/data_sheets/ds890-ultrascale-overview.pdf